IBM Field Engineering
Maintenance Diagrams

1130 Computing System Features

Y26-4003-3

PREFACE

This manual contains maintenance diagrams for the following features of the IBM 1130 Computing System:

Synchronous Communications Adapter
IBM 2501 Card Reader Adapter
IBM 1231 Optical Mark Page Reader Adapter

Use the system diagrams at the engineering level of the equipment being serviced when there is a difference between the system diagrams and the maintenance diagrams in this manual.

Fourth Edition (May 1970)

This manual is a complete revision of SY26-4003-2 and obsoletes the previous edition.

Specifications contained herein are subject to change from time to time. Any such change will be reported in subsequent revisions or Field Engineering Supplements.

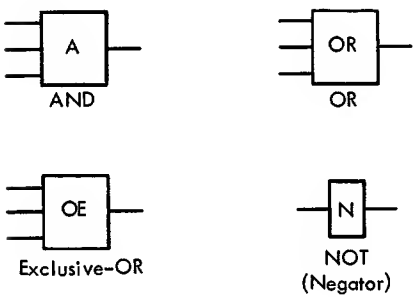
Copies of this and other IBM publications can be obtained through IBM Branch Offices.

A form for readers' comments is provided at the back of this publication. If the form has been removed, send your comments to IBM Corporation, General Systems Division, Product and Programming Publications, Boca Raton, Florida, 33432.

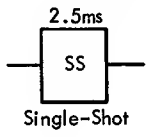
LEGEND

In positive logic representotion, signol levels ore disregorded. The negotor (N block symbol) is used to invert logic, not level. Possive elements (such os drivers ond pulse shopers) generolly ore not shown, since they cantribute nathing to the logic.

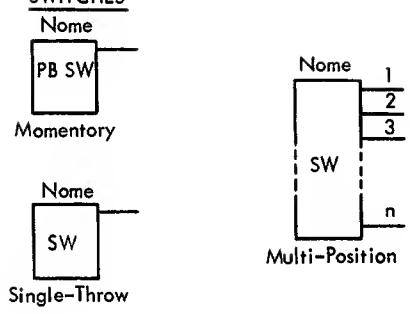
LOGICAL ELEMENTS



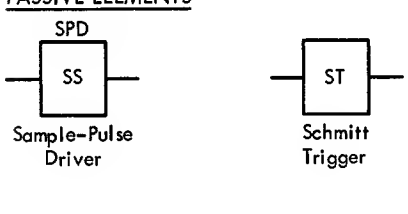
TIMING ELEMENTS

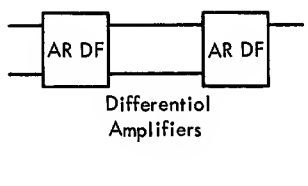


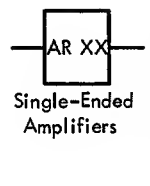
SWITCHES



PASSIVE ELEMENTS



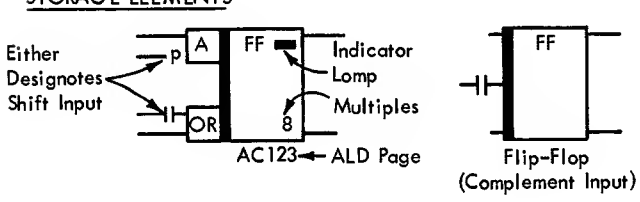


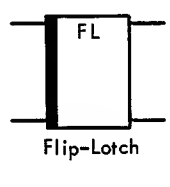


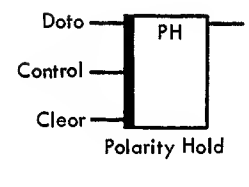
XX Abbreviotions

V = Voltoge Amplifier
LD = Line Driver
LT = Line Terminotor
MD = Magnet Driver
HD = Head Driver
ID = Indicotor Driver
CD = Core Driver

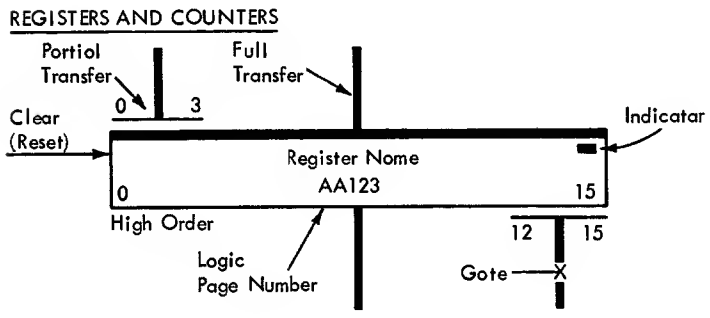
STORAGE ELEMENTS

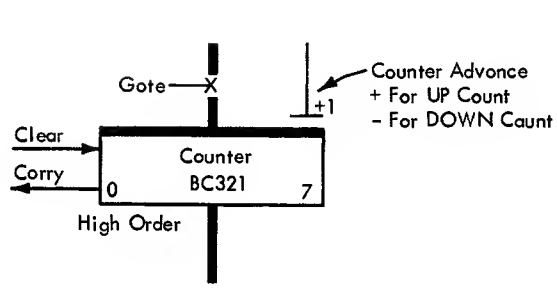






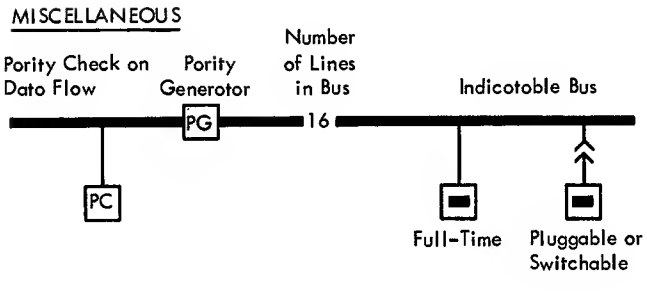
REGISTERS AND COUNTERS

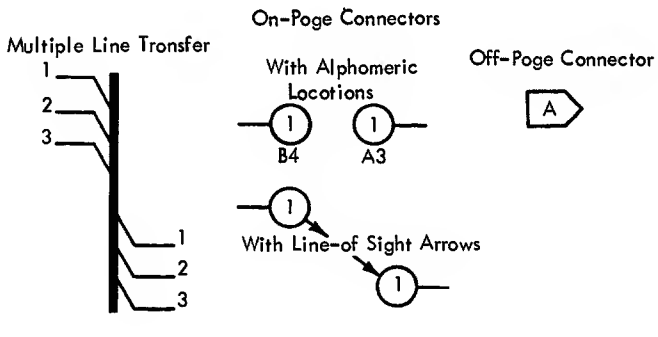




SHIFT REGISTERS

MISCELLANEOUS





A

B

C

D

E

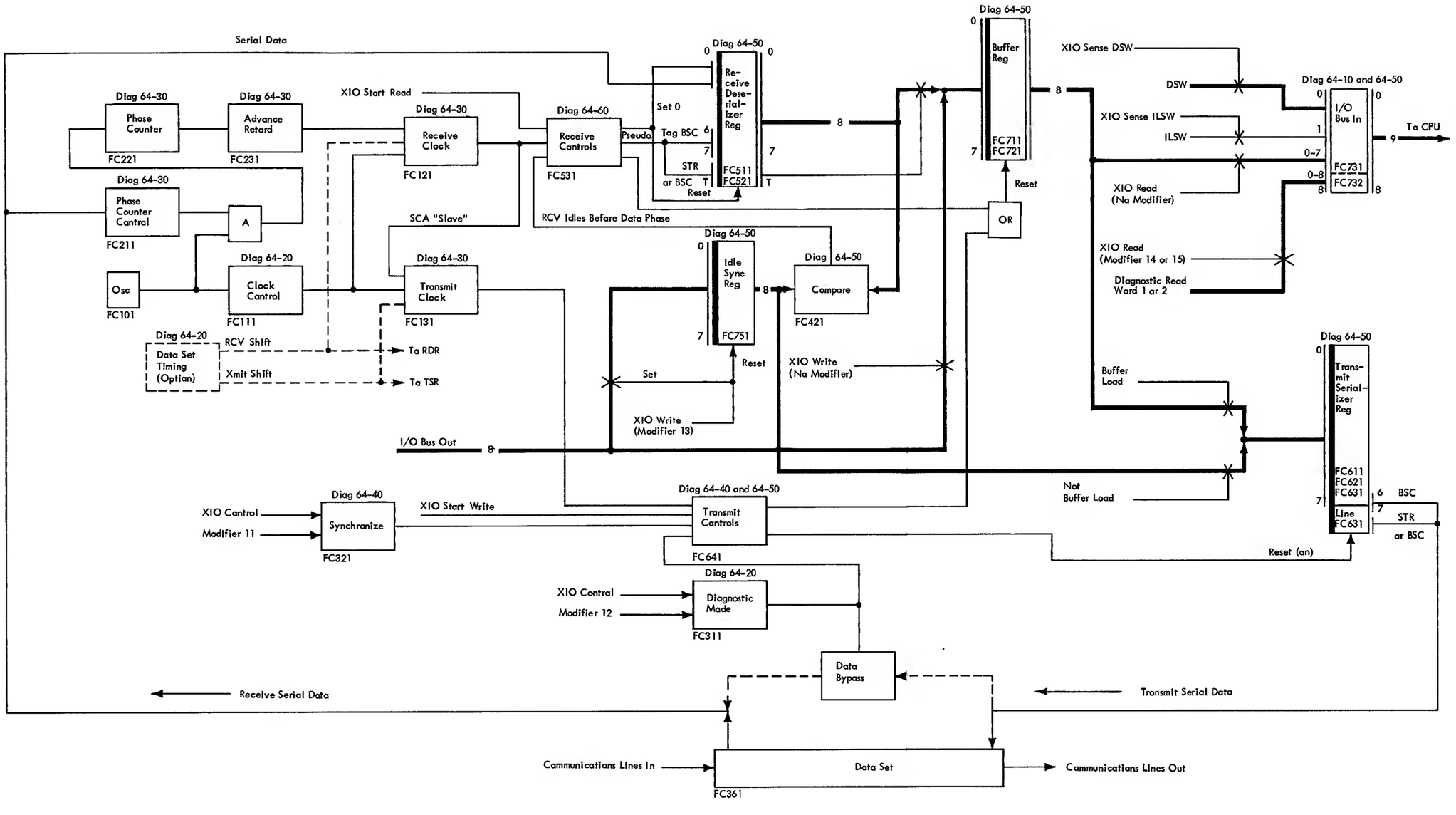


Diagram 63-10. SCA Data Flow and Cantral

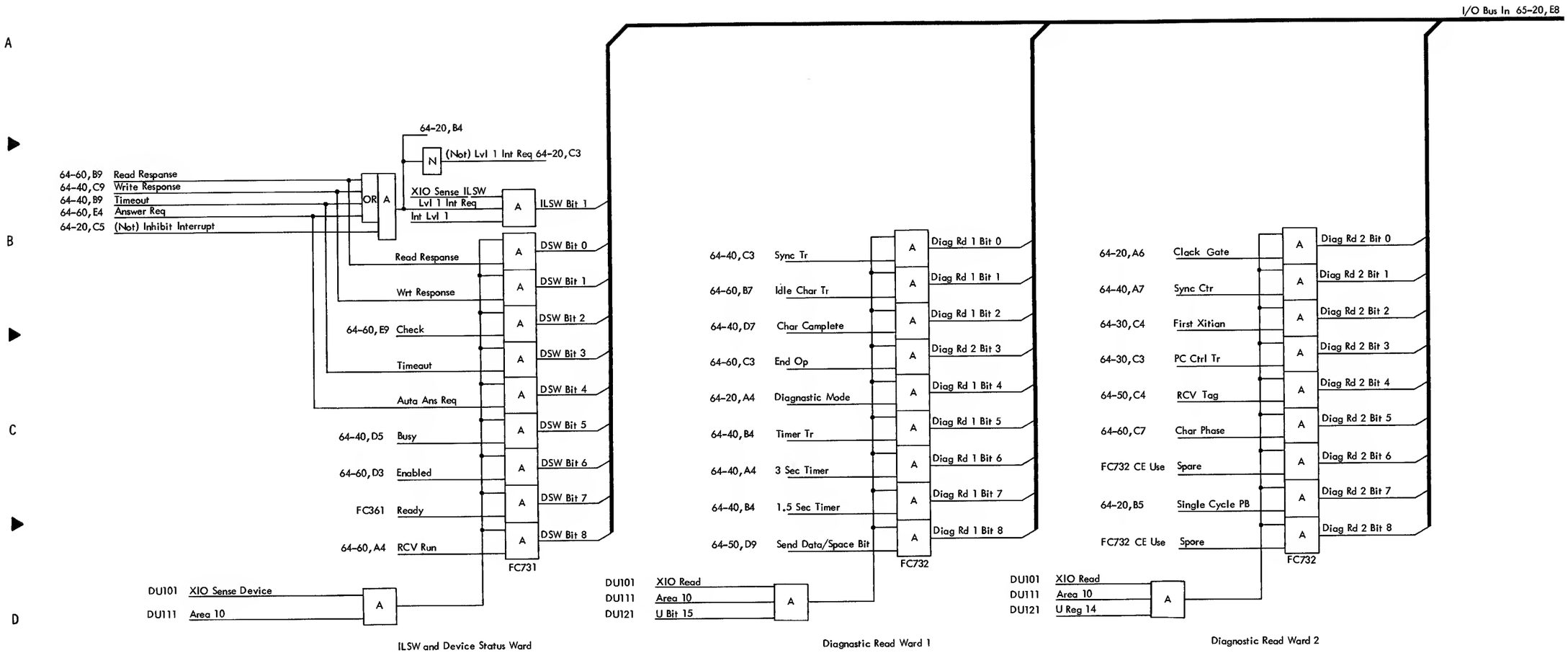
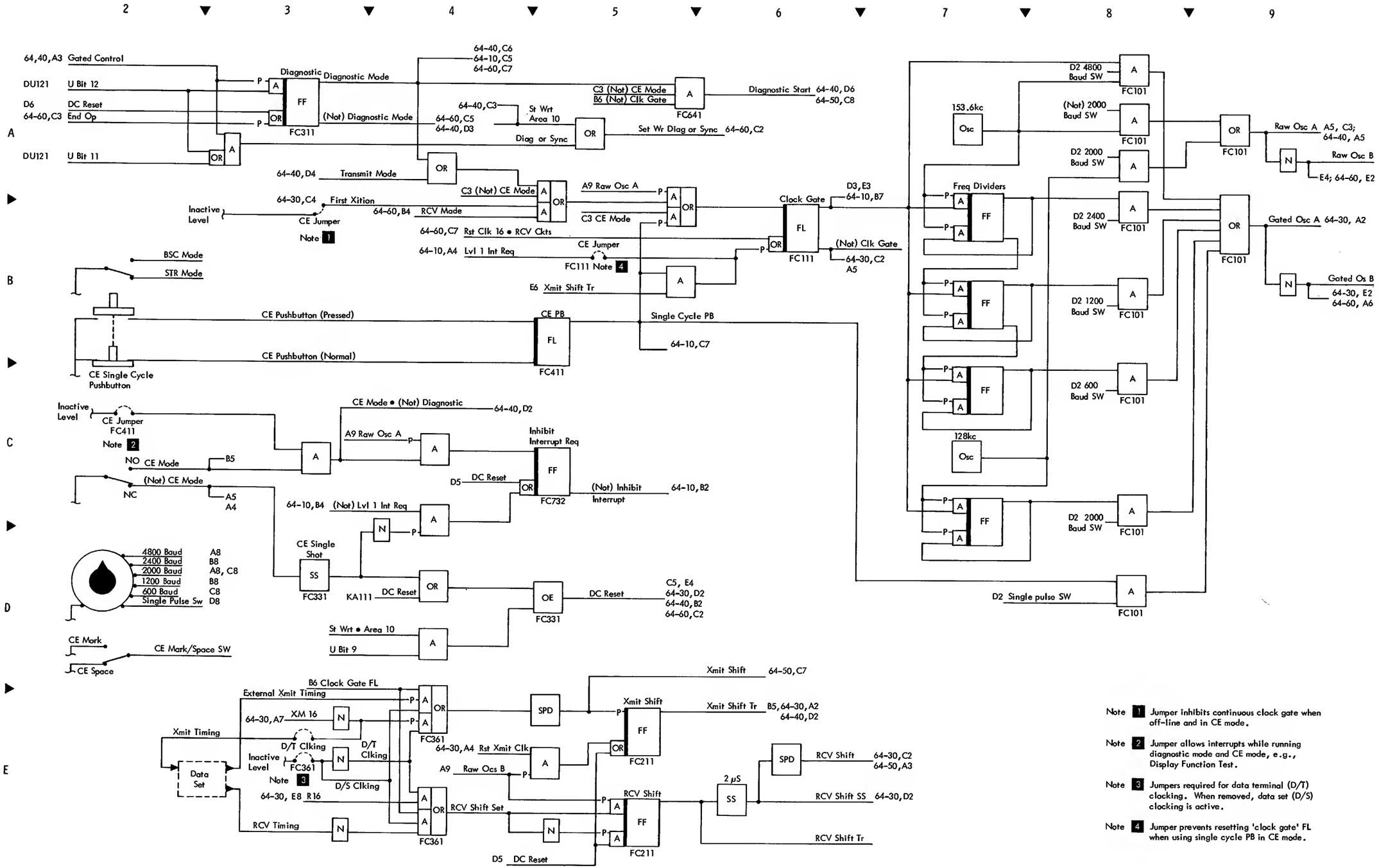


Diagram 64-10. DSW and Diagnostic Read Words 1 and 2

Diagram 64-20. Clock Controls, CE Mode and Switches, and Diagnostic Mode



Note 1 Jumper inhibits continuous clock gate when off-line and in CE mode.

Note 2 Jumper allows interrupts while running diagnostic mode and CE mode, e.g., Display Function Test.

Note 3 Jumpers required for data terminal (D/T) clocking. When removed, data set (D/S) clocking is active.

Note 4 Jumper prevents resetting 'clock gate' FL when using single cycle PB in CE mode.

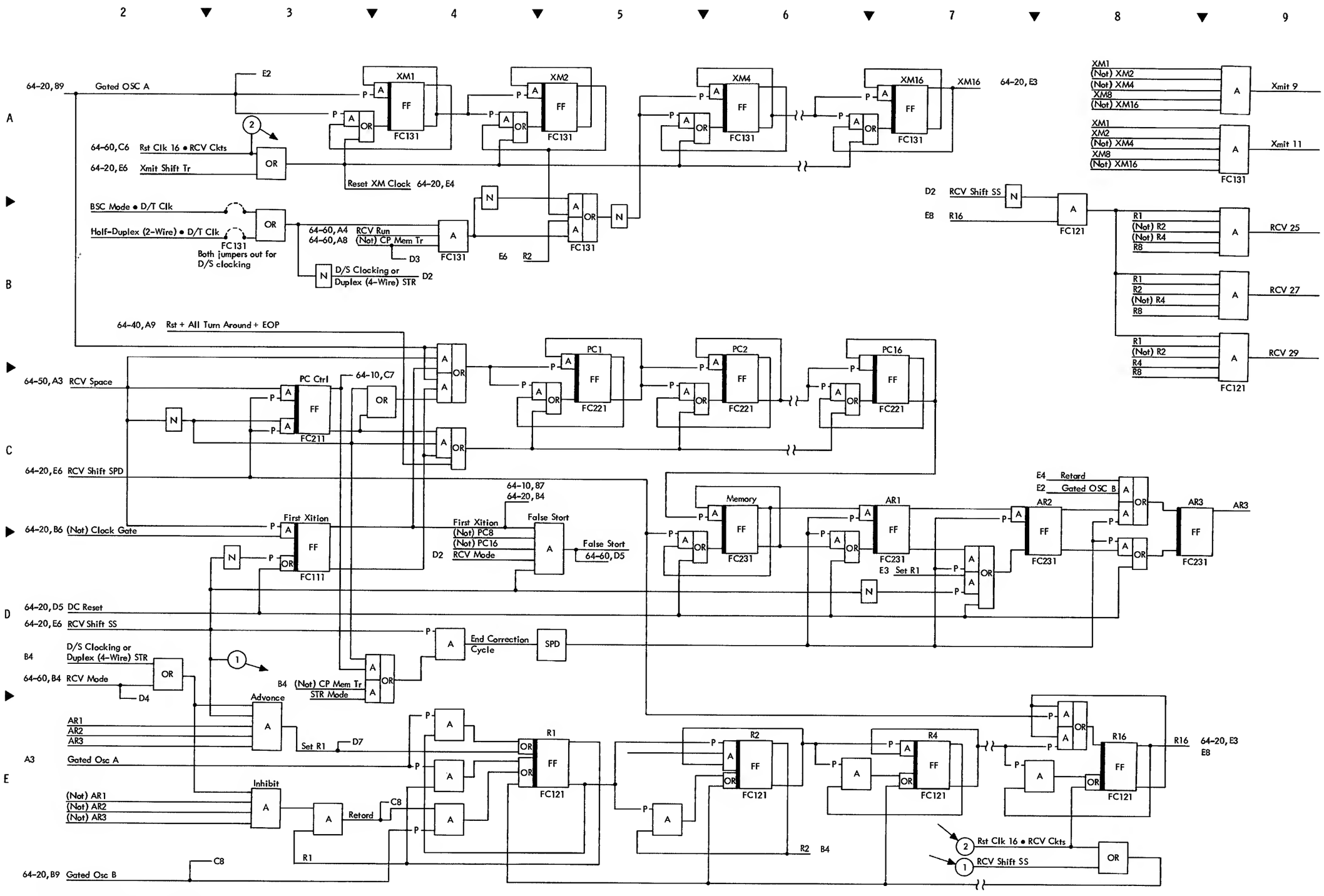
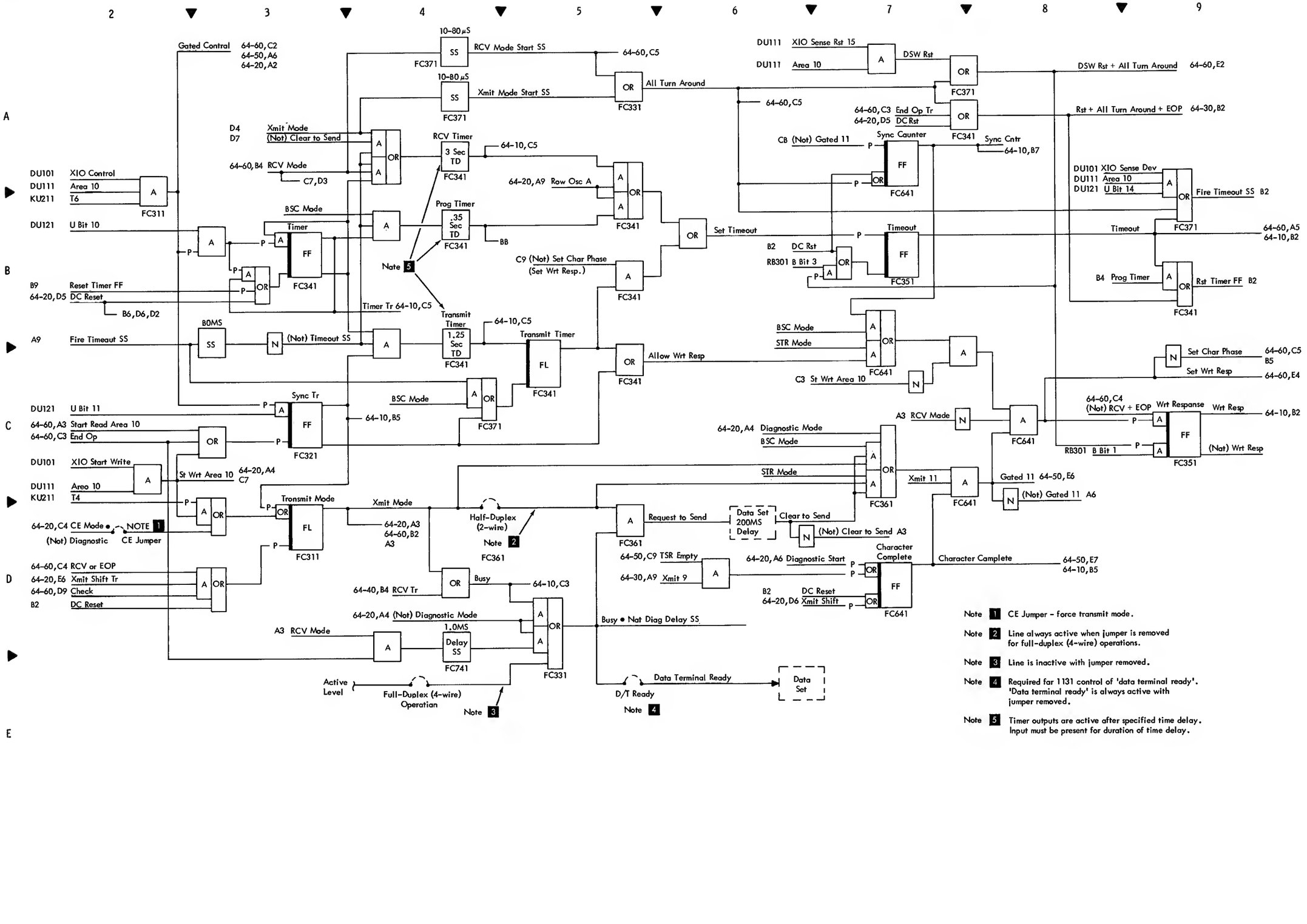


Diagram 64-30. Clocks, Phase Counter, and Advance/Retard

Diagram 64-40. Synchronize and Start Write



Note 1 CE Jumper - force transmit mode.

Note 2 Line always active when jumper is removed for full-duplex (4-wire) operations.

Note 3 Line is inactive with jumper removed.

Note 4 Required for 1131 control of 'data terminal ready'. 'Data terminal ready' is always active with jumper removed.

Note 5 Timer outputs are active after specified time delay. Input must be present for duration of time delay.

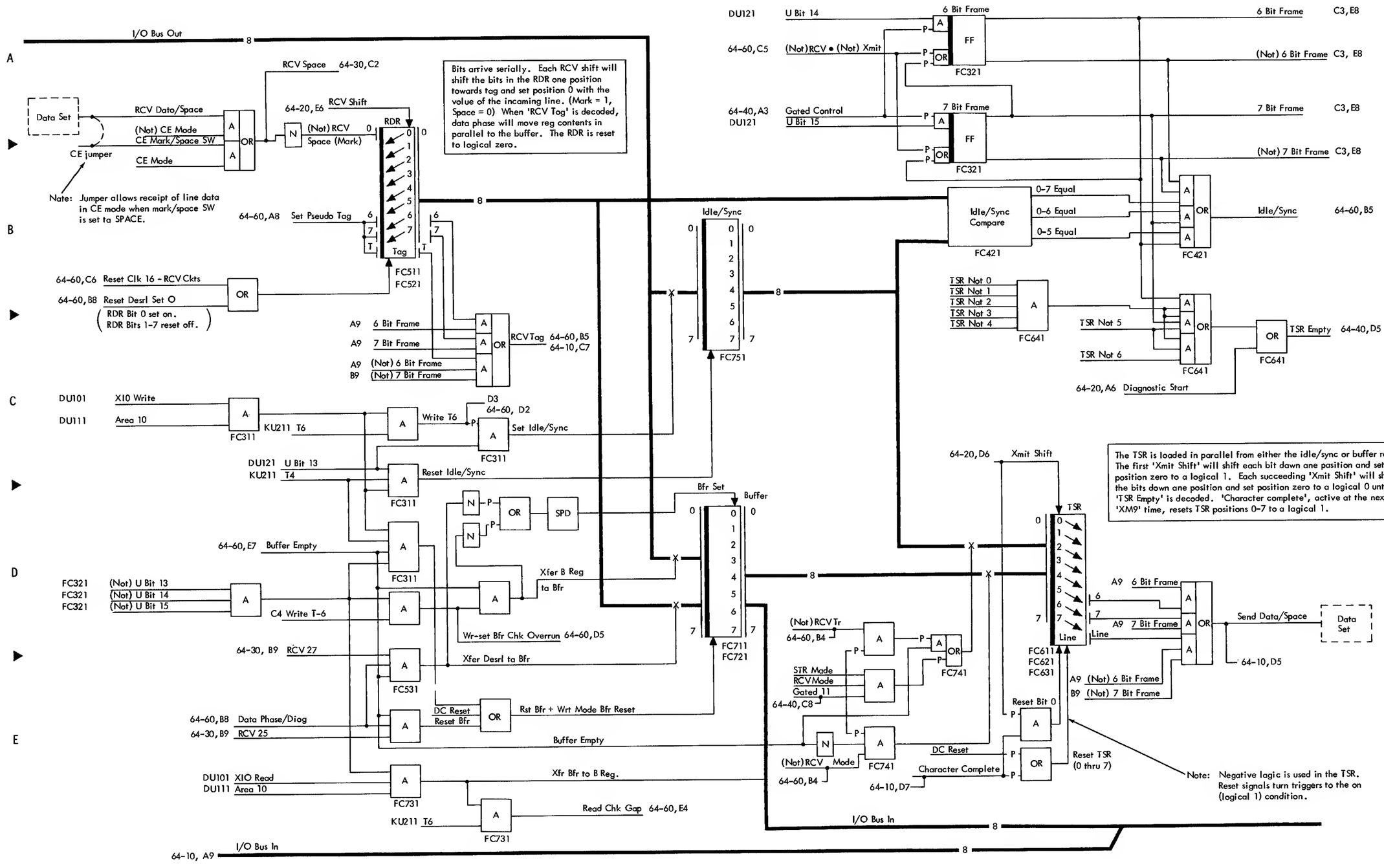


Diagram 64-50. Read and Write

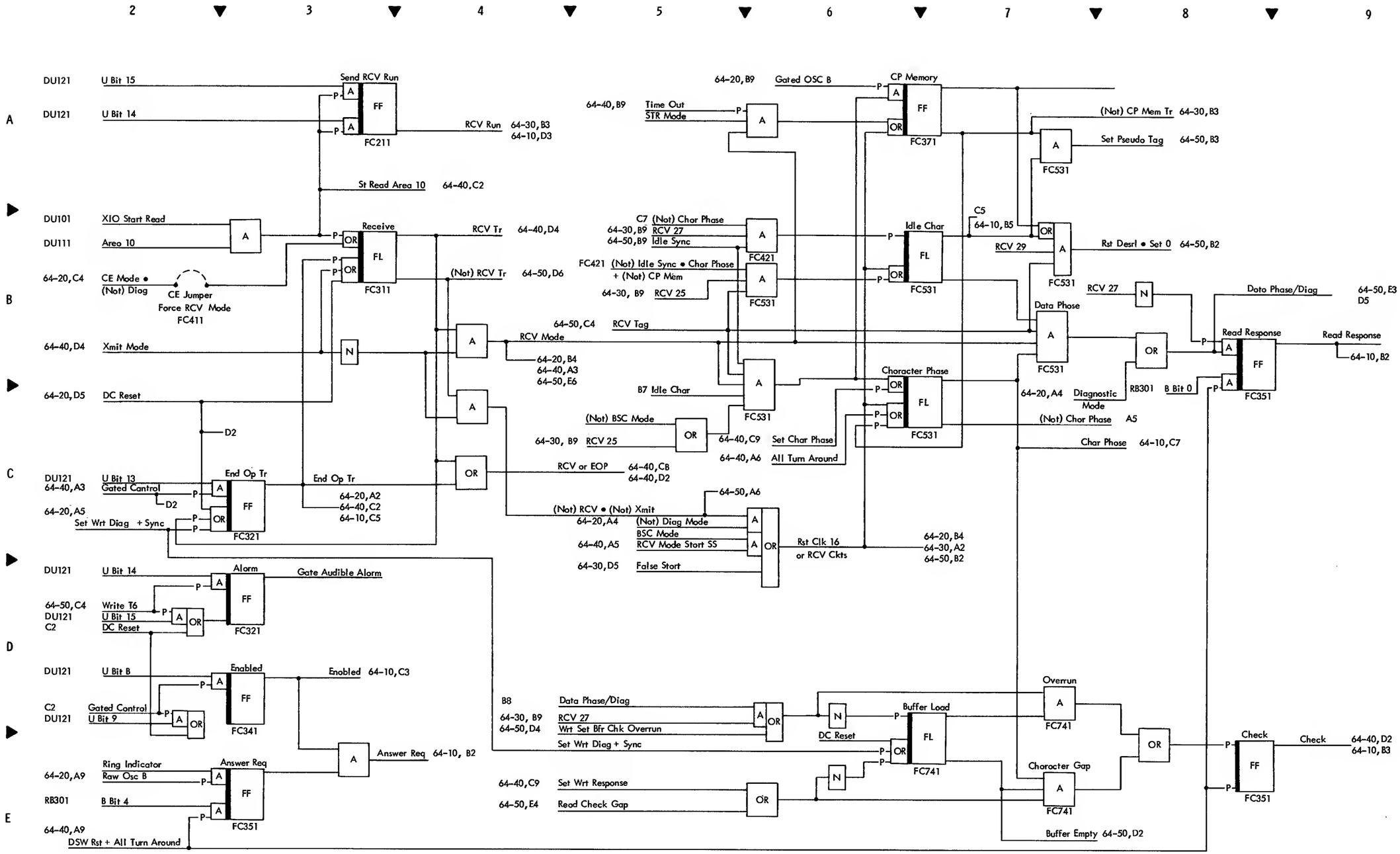


Diagram 64-60. Start Read and Checks

Diagram 65-10. Synchranize, Start Write, and Write (Objectives and Operation)

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

'Synchranize' Objectives - STR

1. Transmit cantents af idle-sync register repeatedly.
2. Black write responses far 1.25 sec.
3. When write responses are allawed, cantinue transmitting characters fram CPU care starage under pragram cantral.

'Synchranize' Operatian - STR (64-40)

1. Turn an 'synchronize trigger' FF (C3) and 'transmit' FL (D3) and reset aff the 'buffer laad' FL (64-60, D7).
2. Start 1.25 sec timer (B4) and fire transmit made start SS (A4).
3. Start clacks, if nat already started (64-20, A4).
4. Activate 'request to send' line (D5) if nat already active. In full duplex (4-wire), this accurs when the SCA first becomes busy and is nat in diagnastic mode.
5. After about 200 ms, data set activates 'clear to send', if nat already active. 'Clear ta send' remains active as lang as 'request ta send' remains active.
6. With TSR empty, at 'Xmit 9', turn an 'character camplete' (D6).
7. At 'gated 11', attempt ta set 'write respanse' but cannat (C8).
8. With buffer empty, at 'gated 11', transfer sync register ta TSR (64-50, E6).
9. Repeat steps 6, 7, and 8 until 1.25 sec timer times aut.
10. Turn on 'transmit timer' latch (C5). Allaw write responses until turned aff.
11. At the end af the 'gated 11' which sets write response the first time, turn an 'character phase' FF (64-60, C6).
12. With the next 'start read write end ap', turn aff 'synchranize trigger' FF. This turns aff the 'Xmit timer latch'.

'Start Write' Objectives - STR

1. Transmit cantents af idle-sync register ance.
2. Start transmitting characters fram CPU core starage under program cantral.

'Start Write' Operatian - STR (64-40)

1. Turn an 'transmit' FL (D3), activating transmit mode. Reset 'buffer laad' FL off (64-60, D7).
2. Fire transmit made start SS (A4), activating 'all turn around'.
3. Reset cantrals far other operatian, such as 'receive' ar 'end ap' (64-60, B2, C2). Turn aff 'char phase' FL, but nat 'CP Mem' FF (64-60, C6).
4. In half duplex (2-wire) system, activate 'request ta send' (D5). In full duplex (4-wire) system, 'request to send' is always active.
5. Approximately 200 ms after 'request ta send' is activated, data set activates 'clear to send', which remains active as lang as 'request ta send', is active.
6. With TSR empty, at 'Xmit 9', turn an 'character camplete' (D6).
7. At 'gated 11', set write response (C9), which causes interrupt level 1 (64-10, B3). (Character gap check is inhibited because 'character phase' is off.)
8. With buffer empty, at 'gated 11', transfer sync reg to TSR (64-50, E6). At end af first 'gated 11', turn on 'character phase' (64-60, C6).
9. While the ane idle-sync character is being transmitted, program must load buffer register with next character from CPU care starage, ta prevent 'character gap'.
10. At each 'character camplete' set 'write response' and interrupt. Check far 'character gap' (64-60, E7).
11. While each character is being transmitted, pragram must load buffer register with next character.
12. Shauld 'character gap' accur, laad TSR fram the idle-sync register.
13. When the program recognizes that the last character has been transferred ta the buffer register, a 'start read' instructian is usually given.
14. With 'receive' FL an, block 'Xfer sync reg ta Xmit ser' until 'RCV mode' becomes active (64-60, B4). (In 4-wire STR, these transfers are necessary during receive mode.)
15. 'Character gap' check is set at 'set write respanse' time when the last bit af the last character is in the line positian af the TSR, 'TSR empty' (64-50, C9).
16. 'Xmit shift tr' becaming active again turns aff the 'transmit' FL (D3) and activates 'receive made' (64-60, B4).

'Synchronize' Objectives - BSC

1. Transmit contents af idle-sync register at least twice.
2. Black ane write response.
3. When write responses are allawed, continue transmitting characters fram CPU care starage under program cantrol.
4. If still transmitting after 1.25 sec, cause timeaut interrupt.

'Synchranize' Operatian - BSC (64-40)

1-8. Same as 'Synchronize' Operatian - STR.
9. At end af first 'gated 11', turn on 'sync caunter' FF (A7). This 'gated 11' cannot 'set write response' because 'sync counter' is off.
10. At each fallawing 'gated 11' set 'write response' (C9).
11. At the end af the 'gated 11' which sets write response the first time, turn on 'character phase' FF (64-60, C6).
12. Cantinue transmitting as in steps 10-16 af 'start write' aperatian - STR.
13. With next 'start read write end ap', turn off 'synchranize trigger' FF (C3).
14. If the next instruction does nat accur befare 1.25 sec have elapsed, turn an 'Xmit timer latch' and set 'timeaut' FF (B7) when the next 'set write response' occurs, causing an interrupt.
15. The pragram can use the interrupt to insert 'sync' characters in the transmitted data.
16. The program con cause a timeaut interrupt after 0.35 sec by an instructian which turns an the pragram timer (B4).

'Start Write' Objectives - BSC

1. Transmit cantents af idle-sync register twice.
2. Start transmitting characters fram CPU care storage under program cantral.

'Start Write' Operatian - BSC (64-40)

1-6. Same as 'Start Write' Operatian - STR.
7. At first 'gated 11', prevent setting 'write respanse' (C9). With buffer empty, transfer idle-sync register ta TSR (64-50, D7).
8. At end af first 'gated 11', turn on 'sync caunter' FF (A7).
9. At secand 'gated 11', set 'write respanse', which causes interrupt level 1 (64-10, B3).
10. At secand 'gated 11' again transfer idle-sync reg to TSR. At end af this 'gated 11', turn an 'character phase' FF (64-60, C6).
11. While secand idle-sync character is being transmitted, pragram must laad buffer with next character from CPU core starage.
12. Cantinue as in steps 10-16 af 'Start Write' Operation - STR. Hawever, in step 14, the 'Xfer sync reg ta Xmit ser' line is nat reactivated in receive mode (64-50, E6).

'Write' Objectives - STR ar BSC

1. Check far overrun.
2. Load buffer register with next character fram CPU care starage.

'Write' Operatian - STR ar BSC (64-50)

1. At T4 of CPU E-3 cycle, if 'buffer load' FL is off (64-60, E7), reset buffer register (D5). ('Buffer laad' aff indicates previaus character has read aut, and 'buffer empty' is active.
2. At T6, if 'buffer load' FL is an, turn an 'check' FF (Overrun).
3. At T6, if 'buffer load' FL is aff, gate 'transfer B register ta buffer' (D5).
4. At end af T6, if 'buffer load' FL is aff, activate 'buffer set' SPD (D4) and turn an 'buffer laad' FL (64-60, E6).

'Write-Modifier 13' Objective - STR ar BSC

Load idle-sync register with a character framCPU care starage.

'Write-Modifier 13' Operatian - STR ar BSC (64-50)

1. At T4 af CPU E-3 cycle, with 'U bit 13' active, reset idle-sync register (C4).
2. At T6, with 'U bit 13' active, set idle-sync register from B register autputs (C4).

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

A

'Start Read' Objectives - STR

1. Recognize one idle-sync character and establish 'character phase'.
2. Starting with first non-idle character, receive following characters and set them in buffer register. Idle-sync characters received during 'character phase' are handled as data characters in SCA.

'Start Read' Operation - STR (64-60)

1. Turn on 'receive' FL (B3). If 'transmit' FL is off, activate 'receive mode' immediately. If 'transmit' is on, wait to activate 'receive mode' when 'transmit' turns off.

▶

2. Fire receive mode start SS (64-40, A4). Activate 'all turn around'.
3. Reset controls for other operations. Turn off 'character phase' FL, but not 'CP memory' FF, if they are on (C6 and A6).

B

4. Start receiving and shifting bits through RDR, comparing RDR with idle-sync register (64-50, B3, B7).
5. If 'CP memory' FF is off (not previously in 'character phase', or else a timeout occurred during the last 'receive mode'):
   A. With equal idle-sync compare, turn on 'idle character' FL at RCV 27 (B6).
   B. With 'idle character' on activate 'set pseudo tag' (A7).
   C. Turn on 'character phase' and 'CP memory' (C6 and A6).

▶

6. If 'CP memory' FF is on (previously in 'character phase' and no timeout occurred during the last 'receive mode'):
   A. With equal idle-sync compare, turn on 'idle character' FL at RCV 27 (B6).

C

   B. Framing was previously completed (tags shifting through RDR).
   C. With equal idle-sync compare and 'idle character' on, turn on 'character phase' and 'CP memory' at 'tag' time (A7 and C7).
7. On receipt of the first non-idle character, at 'tag' time turn off 'idle character' at RCV 25 (B5).

▶

8. Activate 'data phase' at RCV tag time (B7).
9. With 'buffer load' off and RCV 25, reset buffer register (64-50, E3).
10. At RCV 27, if 'buffer load' is on, set overrun (D8). If 'buffer load' off, transfer RDR to buffer register (64-50, E4).
11. At end of RCV 27, turn on 'buffer load' FL (D8) and 'read response' FF (B8), activating 'level 1 interrupt request'.

D

12. Continue receiving until 'transmit' or 'end op' instruction turns off 'receive' FL (B3).
13. 'End op' fires the 1.0 ms delay SS to maintain 'busy' for the duration of the SS (64-40, E4).

▶

E

'Start Read' Objectives - BSC

1. Recognize two successive idle-sync characters to establish 'character phase'.
2. Starting with first non-idle character, receive following characters and set them in buffer register.

'Start Read' Operation - BSC (64-60)

1. Turn on 'receive' FL (B3). If 'transmit' FL is off, activate 'receive mode' immediately. If 'transmit' is on, wait to activate 'receive mode' when 'transmit' turns off.
2. Fire receive mode start SS (64-40, A4). Activate 'all turn around' and 'reset clock 16 and RCV circuits' (C5) stopping clocks.
3. Reset controls for other operations. Turn off 'CP memory' FF and 'character phase' FL (A6 and C6).
4. On first mark to space transition, turn on 'clock gate' FL (64-20, B4) restart clocks. Use first transition circuits to ensure no false start from noise. (64-30, D4).
5. Start receiving and shifting bits through RDR, comparing RDR with idle-sync register. When idle-sync compare is equal turn on 'idle character' FL at RCV 27 (B6).
6. Activate 'set pseudo tag' (A7). Framing is complete.
7. If idle-sync compare is equal at the next RCV tag, turn on 'character phase' and 'CP memory' at RCV 25 (C6 and A6).
8. If idle-sync compare is not equal at the next RCV tag turn off 'idle character' FL at RCV 25 (B5). Do not turn on 'character phase' and 'CP memory'.
9. Continue comparison until idle-sync compare is equal when 'idle character' FL is on. Then turn on 'character phase' and 'CP memory' at RCV 25.
10. Continue receive operation as in steps 7-13 of STR.

'Read' Objectives - STR or BSC

1. Check for character gap.
2. Transfer a received character from the buffer register to CPU core storage.

'Read' Operation - STR or BSC (64-60)

1. During CPU E-3 cycle, transfer buffer to B register (64-50, E5).
2. At T6, if the 'buffer load' FL is off during 'character phase', activate 'character gap' and turn on 'check' FF (E7).
3. At the end of T6, turn off 'buffer load' FL (E6).

Diagram 65-20. Start Read and Read (Objectives and Operation)

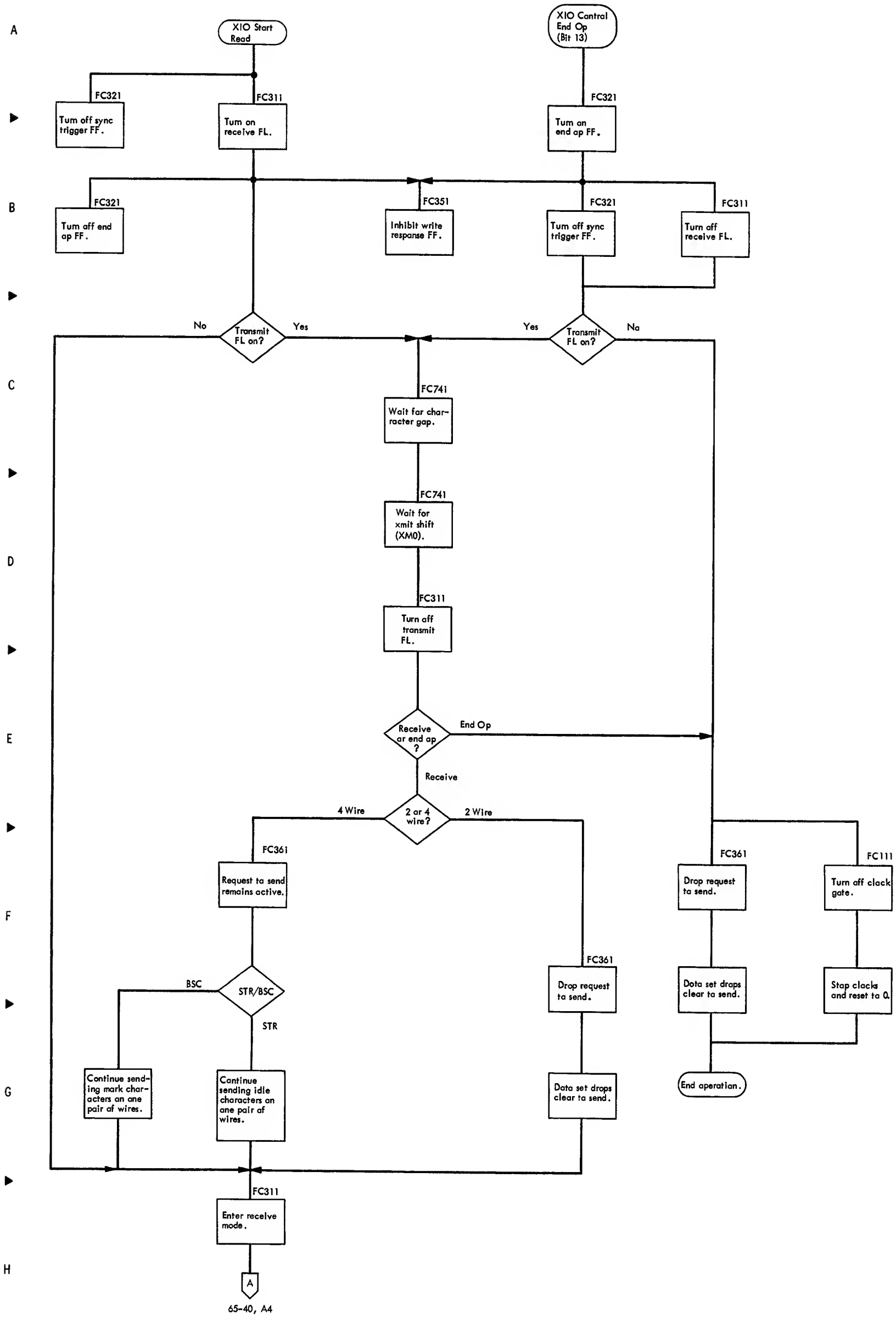


Diagram 65-30. Start Read (Part 1) and End Operation

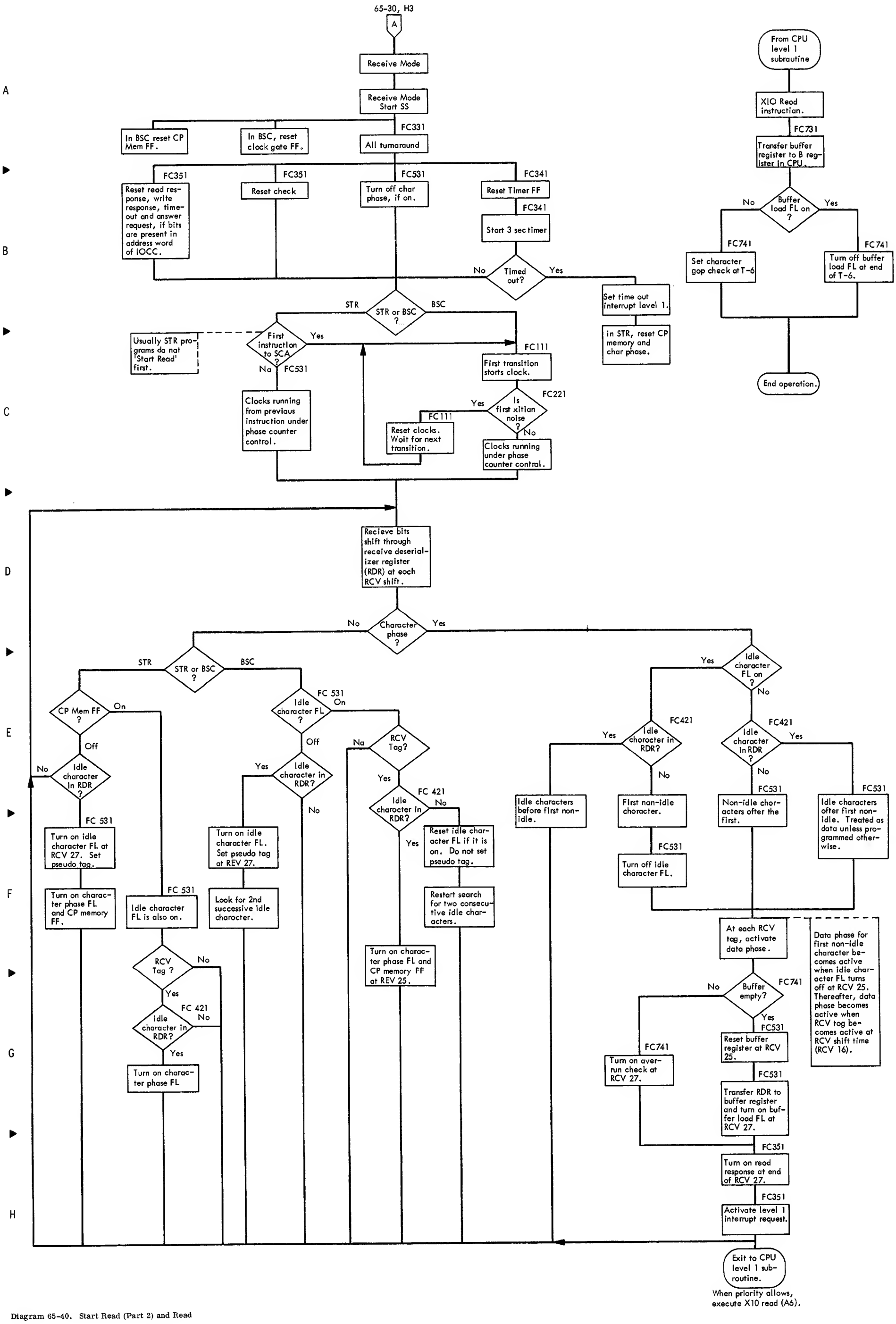


Diagram 65-40. Start Read (Part 2) and Read

A B C D E

2 3 4 5 6 7 8 9

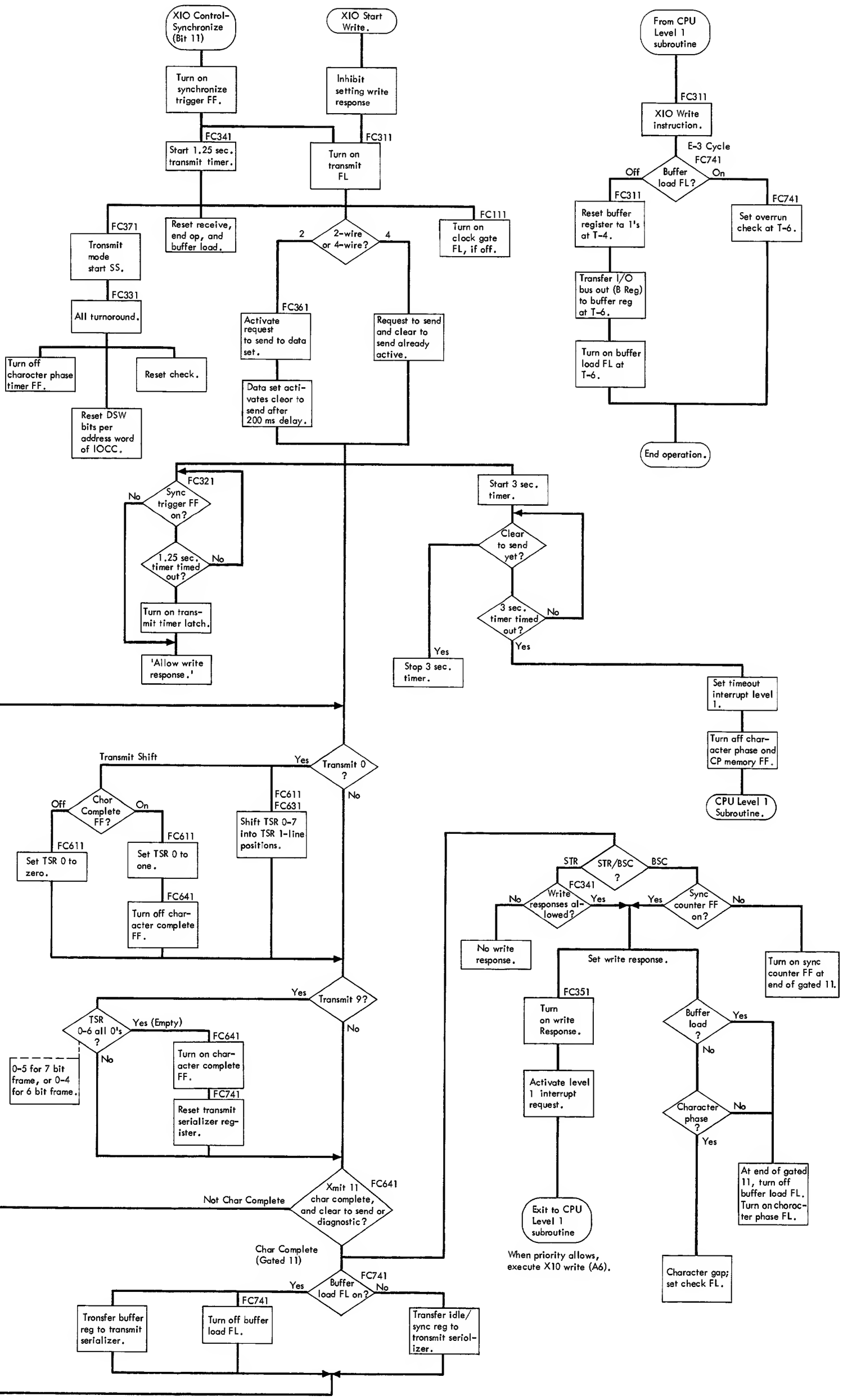
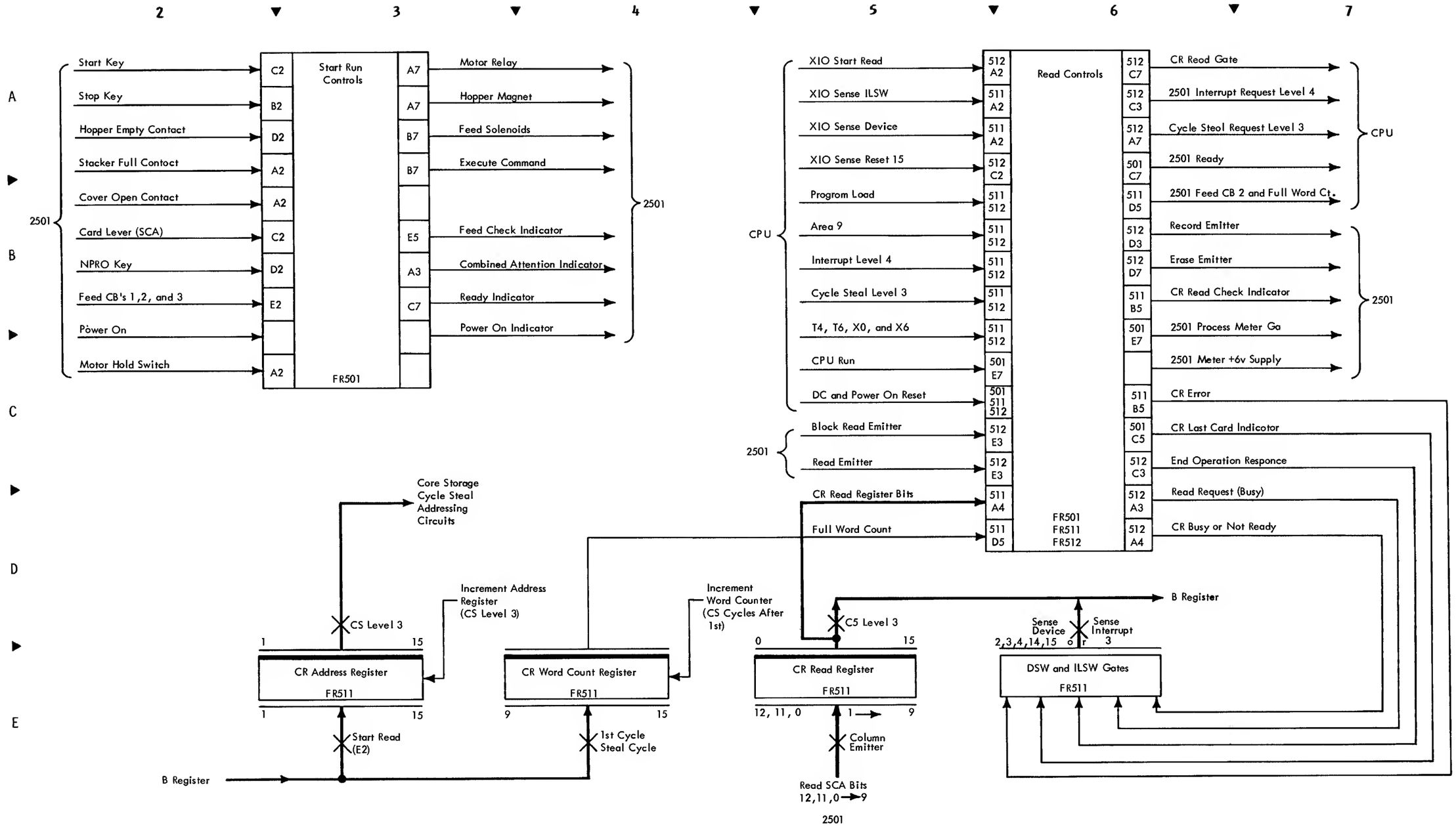


Diagram 65-50. Synchronize, Start Write, and Write


2
3
4
5
6
7
A
B
C
D
E
2501
Start Key
Stop Key
Hopper Empty Contact
Stacker Full Contoct
Cover Open Contact
Card Lever (SCA)
NPRO Key
Feed CB's 1,2, and 3
Power On
Motor Hold Switch
C2
B2
D2
A2
A2
C2
D2
E2
A2
Start Run Controls
FR501
A7
A7
B7
B7
E5
A3
C7
Motor Relay
Hopper Magnet
Feed Solenoids
Execute Command
Feed Check Indicator
Combined Attention Indicator
Ready Indicator
Power On Indicator
2501
CPU
XIO Start Read
XIO Sense ILSW
XIO Sense Device
XIO Sense Reset 15
Progrom Load
Area 9
Interrupt Level 4
Cycle Steal Level 3
T4, T6, X0, and X6
CPU Run
DC and Power On Reset
Block Read Emitter
Read Emitter
CR Read Register Bits
Full Word Count
512 A2
511 A2
511 A2
512 C2
511 512
511 512
511 512
511 512
511 512
501 E7
501 511 512
512 E3
512 E3
511 A4
511 D5
Read Controls
FR501
FR511
FR512
CR Reod Gate
2501 Interrupt Request Level 4
Cycle Steol Request Level 3
2501 Ready
2501 Feed CB 2 and Full Word Ct.
Record Emitter
Erase Emitter
CR Read Check Indicator
2501 Process Meter Ga
2501 Meter +6v Supply
CR Error
CR Last Card Indicotor
End Operation Responce
Read Request (Busy)
CR Busy or Not Ready
CPU
2501
Core Storage Cycle Steal Addressing Circuits
Increment Address Register (CS Level 3)
Increment Word Counter (CS Cycles After 1st)
CS Level 3
C5 Level 3
B Register
Sense Device
Sense Interrupt
2,3,4,14,15
or
3
CR Address Register
FR511
CR Word Count Register
FR511
CR Read Register
FR511
DSW and ILSW Gates
FR511
Start Read (E2)
1st Cycle Steal Cycle
Column Emitter
Read SCA Bits 12,11,0→9
B Register
2501

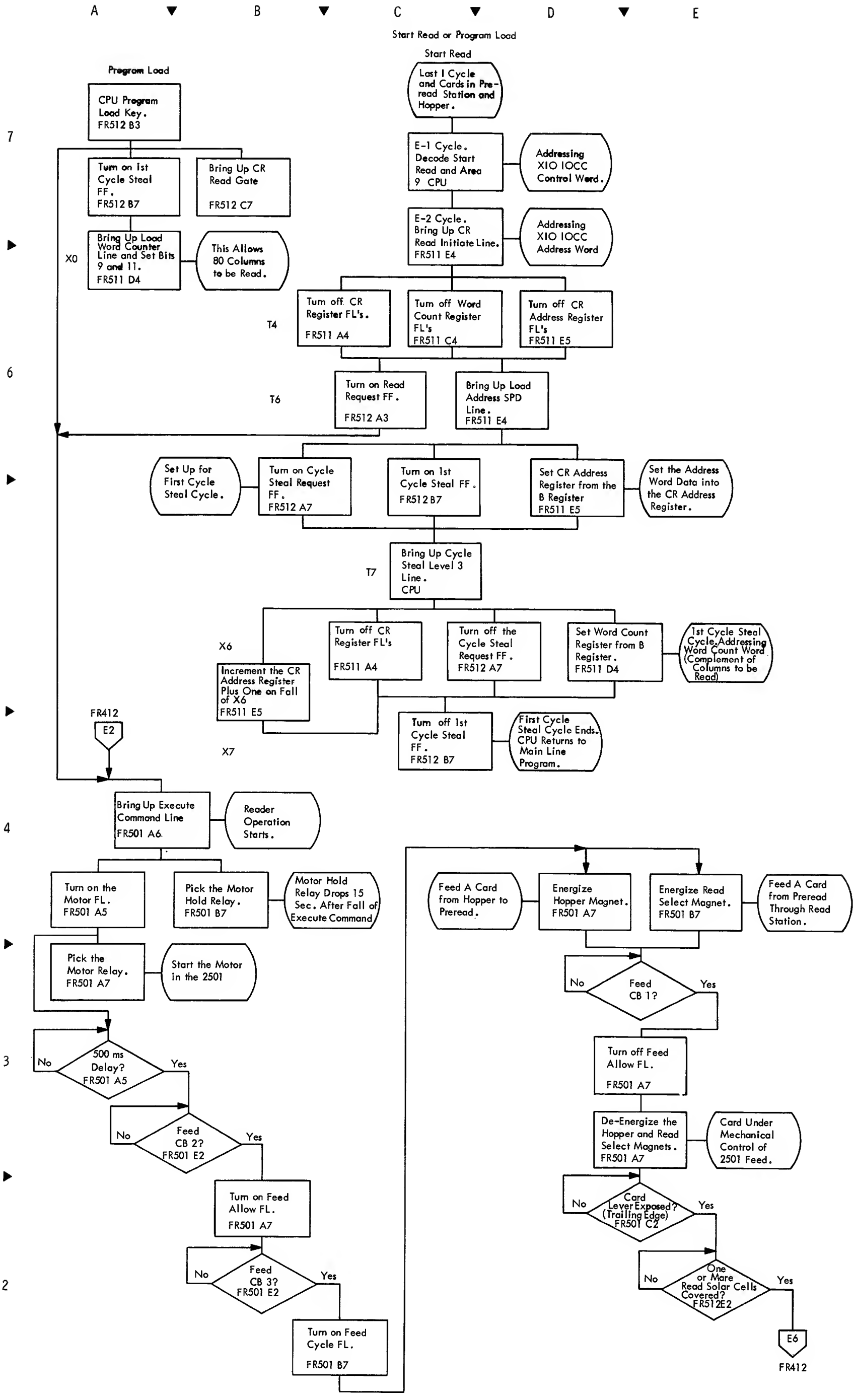


Diagram FR411. 2501 Start Read or Program Load (Part 1 of 2)

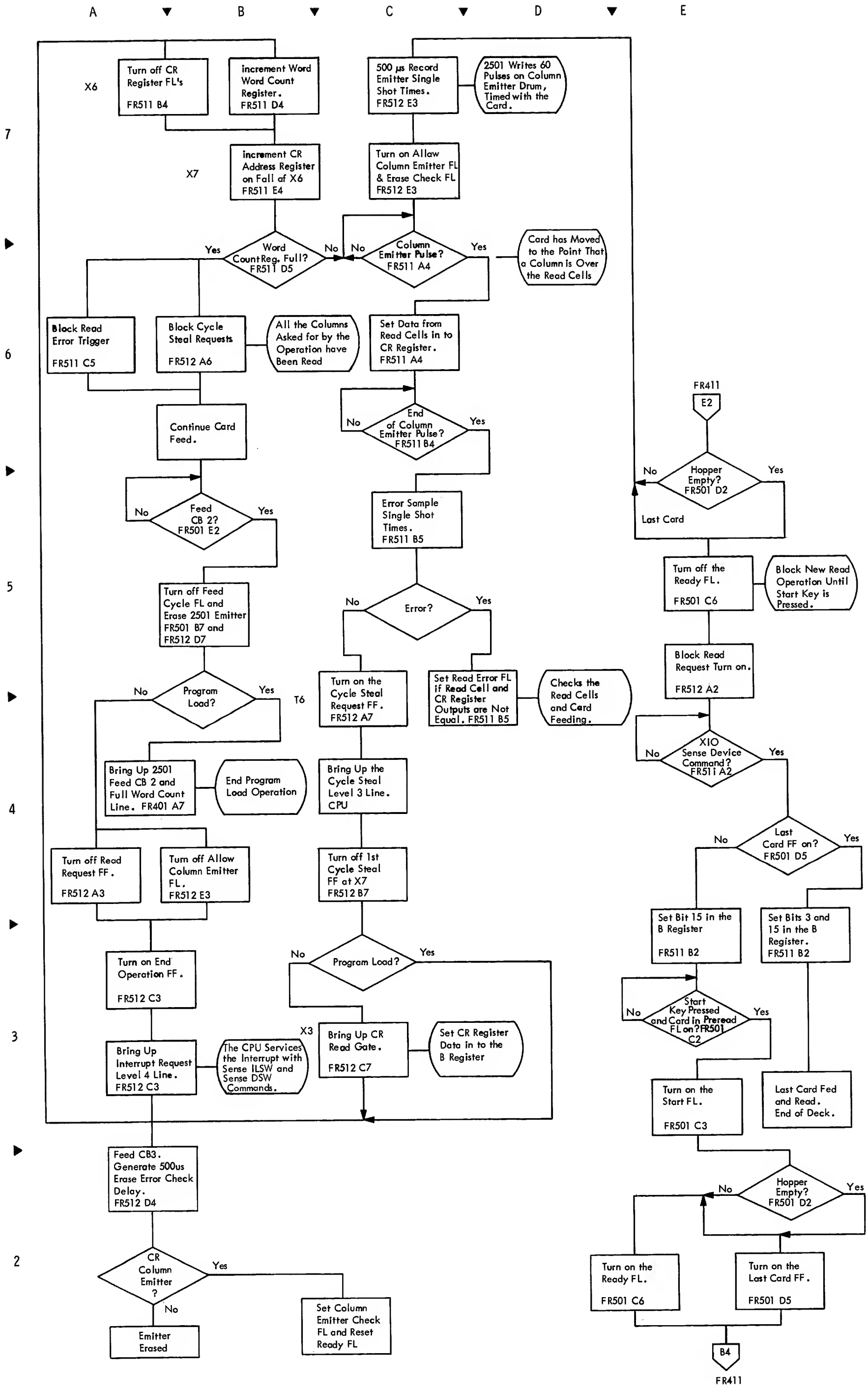


Diagram FR412. 2501 Start Read or Program Load (Part 2 of 2)

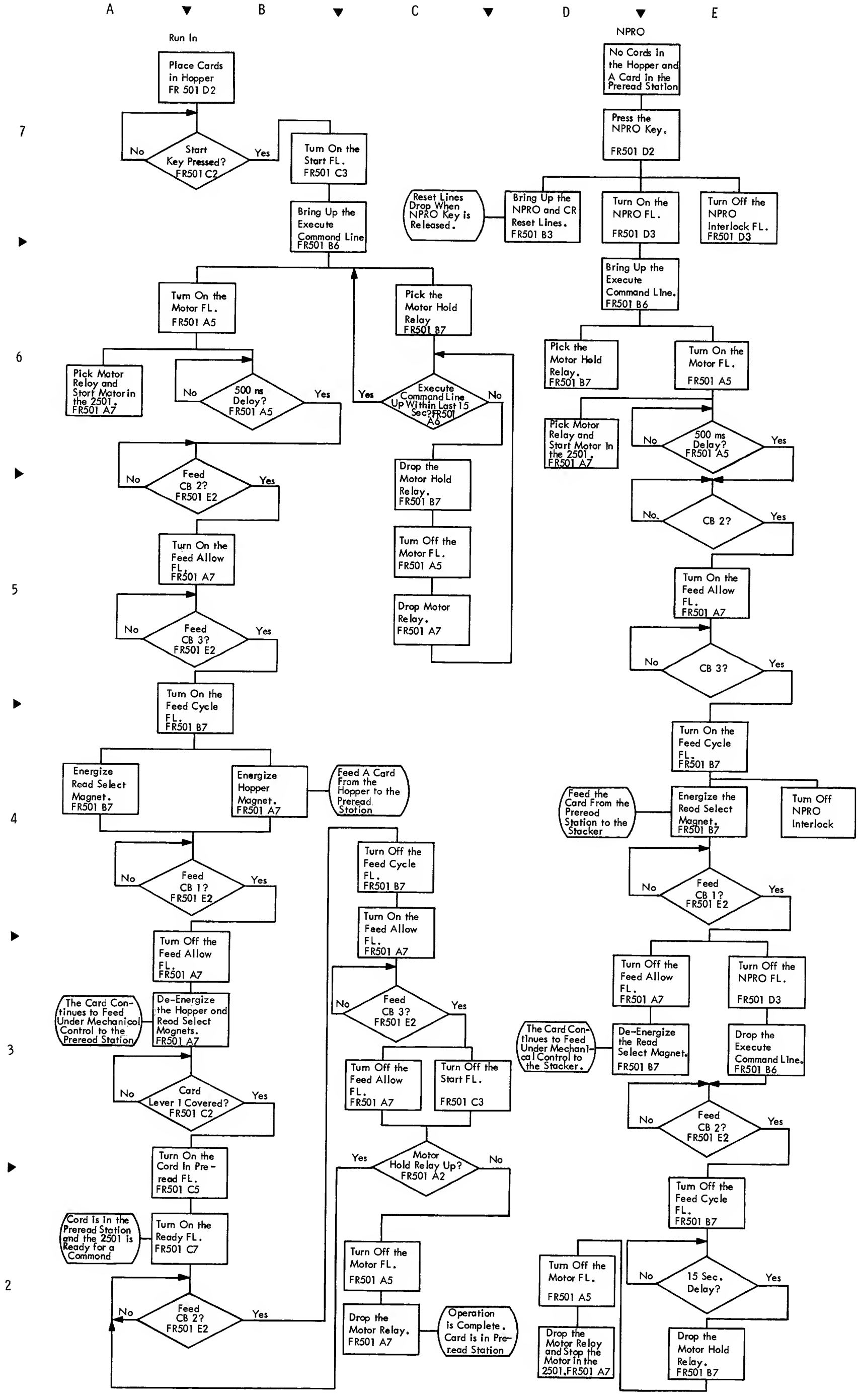


Diagram FR413. 2501 Run In - NPRO

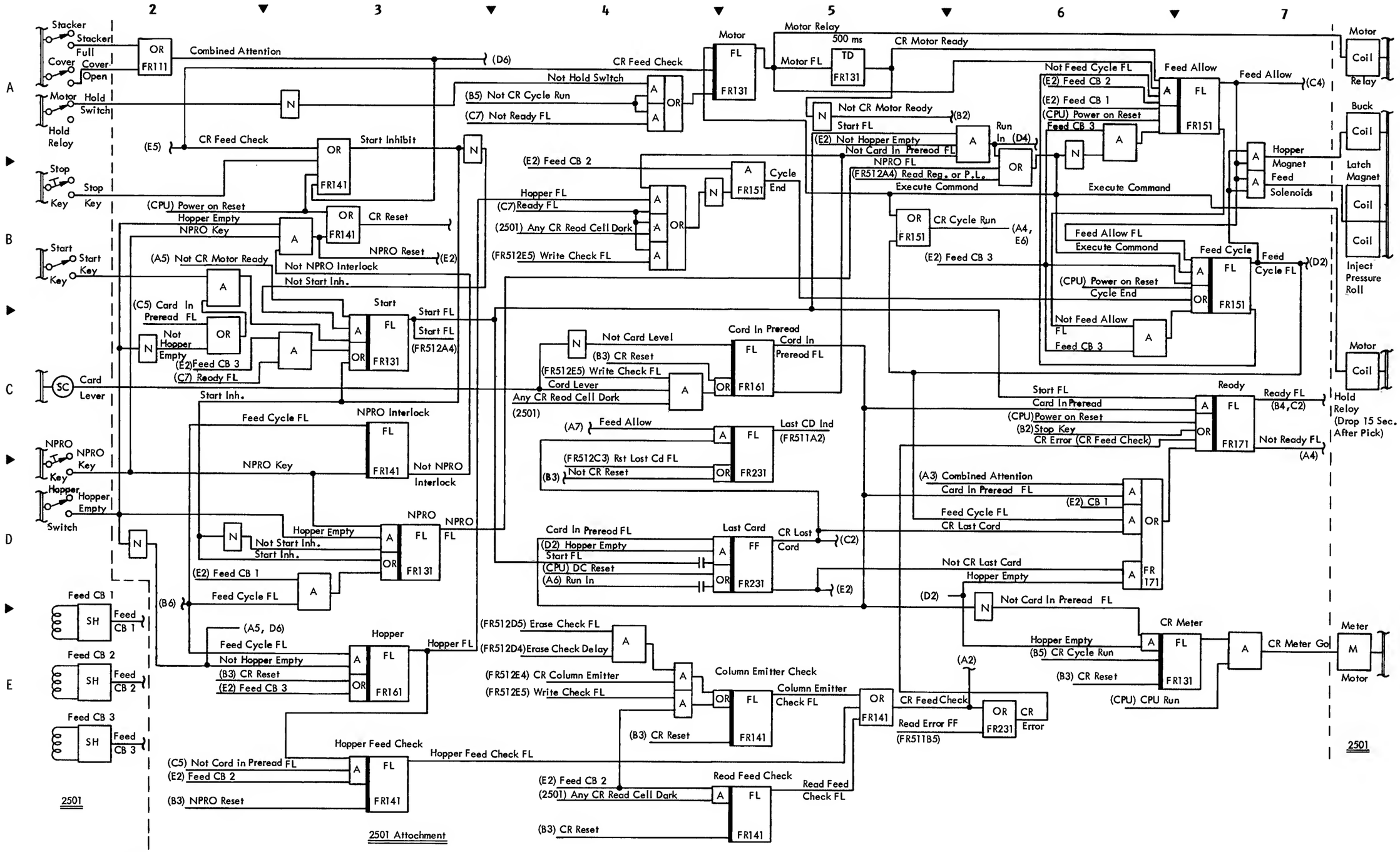
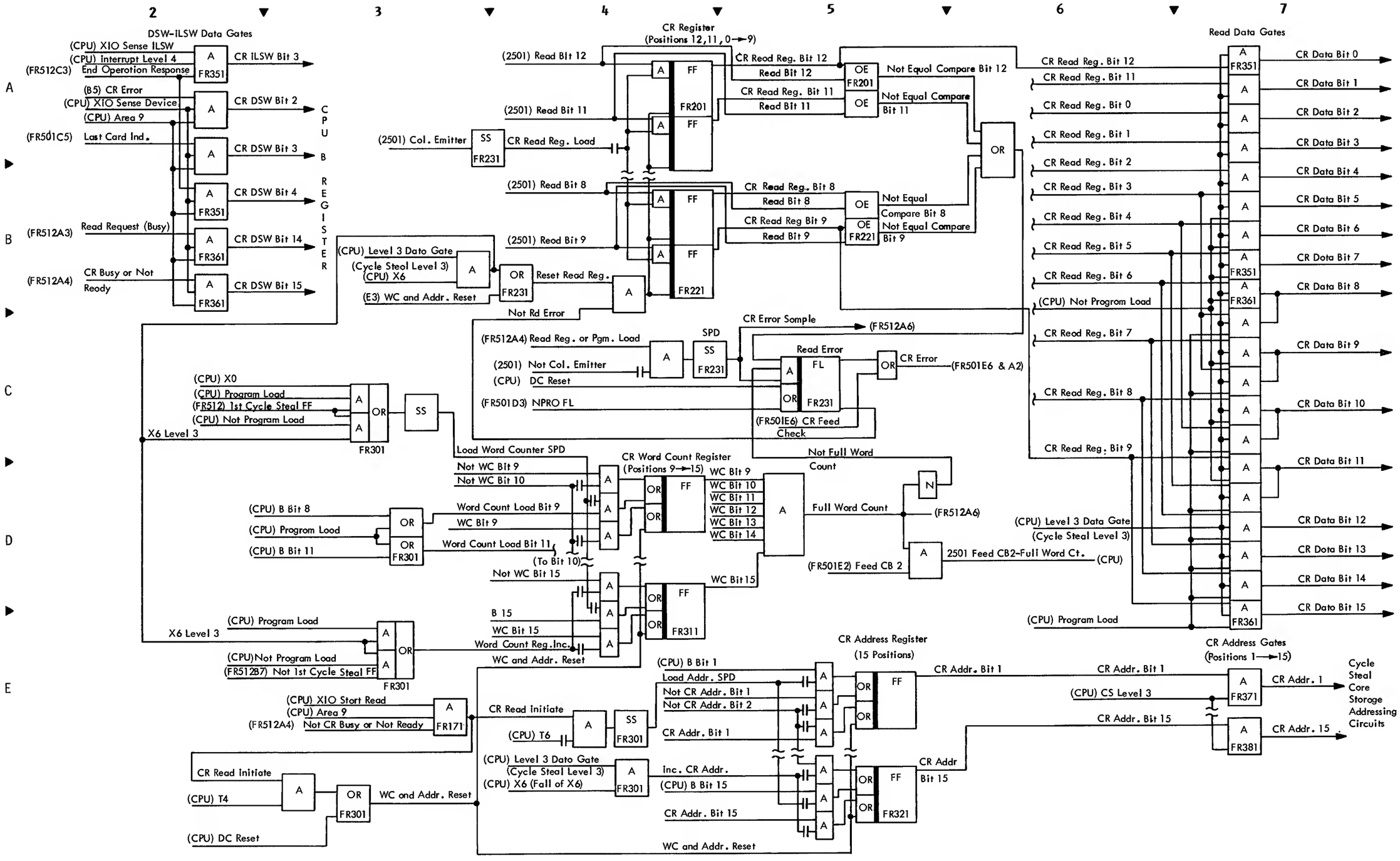


Diagram FR501. 2501 Start-Run

Diagram FR 511. 2501 Read (Part 1 of 2)



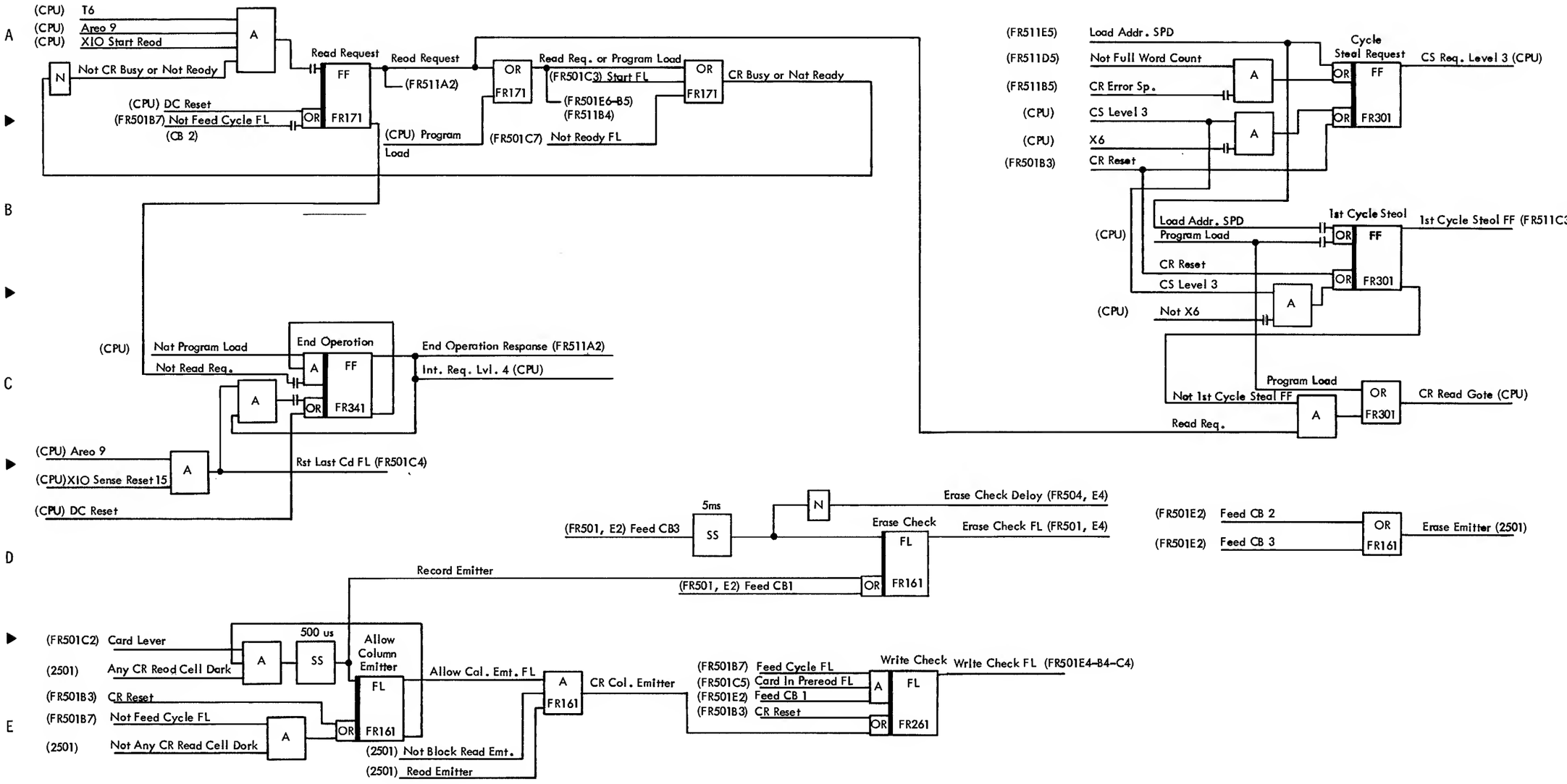
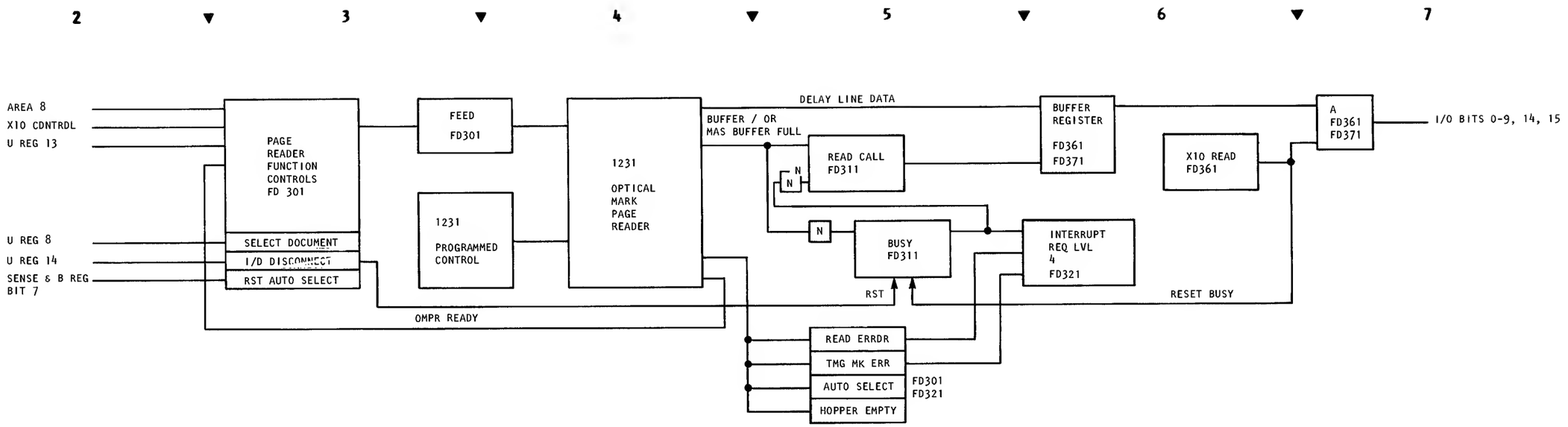


Diagram FR512. 2501 Read (Part 2 of 2)

Diagram 83-10. 1231 Data Flow and Control



B5	DSW AND ILSW BITS FOR 1231	15	OMPR IS NDT READY
C4		14	OMPR READ OP
D6		13	READ BUSY
B7		10	CHECK STOP INT. REQ.
B9		9	OMPR HOPPER IS EMPTY
A9	FD301	8	OMPR TIMING MARK CHECK BUSY
B9	FD311	7	I/D SELECTED DOCUMENT (Auto Select)
B9	FD321	6	OMPR FEED BUSY
A9		5	OMPR OK TO SELECT DOCUMENT (Enable Select)
C6		4	OMPR OPERATION COMPLETE (End Op)
E6		3	MASTER MARK
C2		2	OMPR READ ERROR
C2		1	TIMING MARK CHECK
D6		0	OMPR READ RESPONSE
B9			1231 ILSW BIT 5

Note: References in left column are co-ordinates for Diagram 84-10.

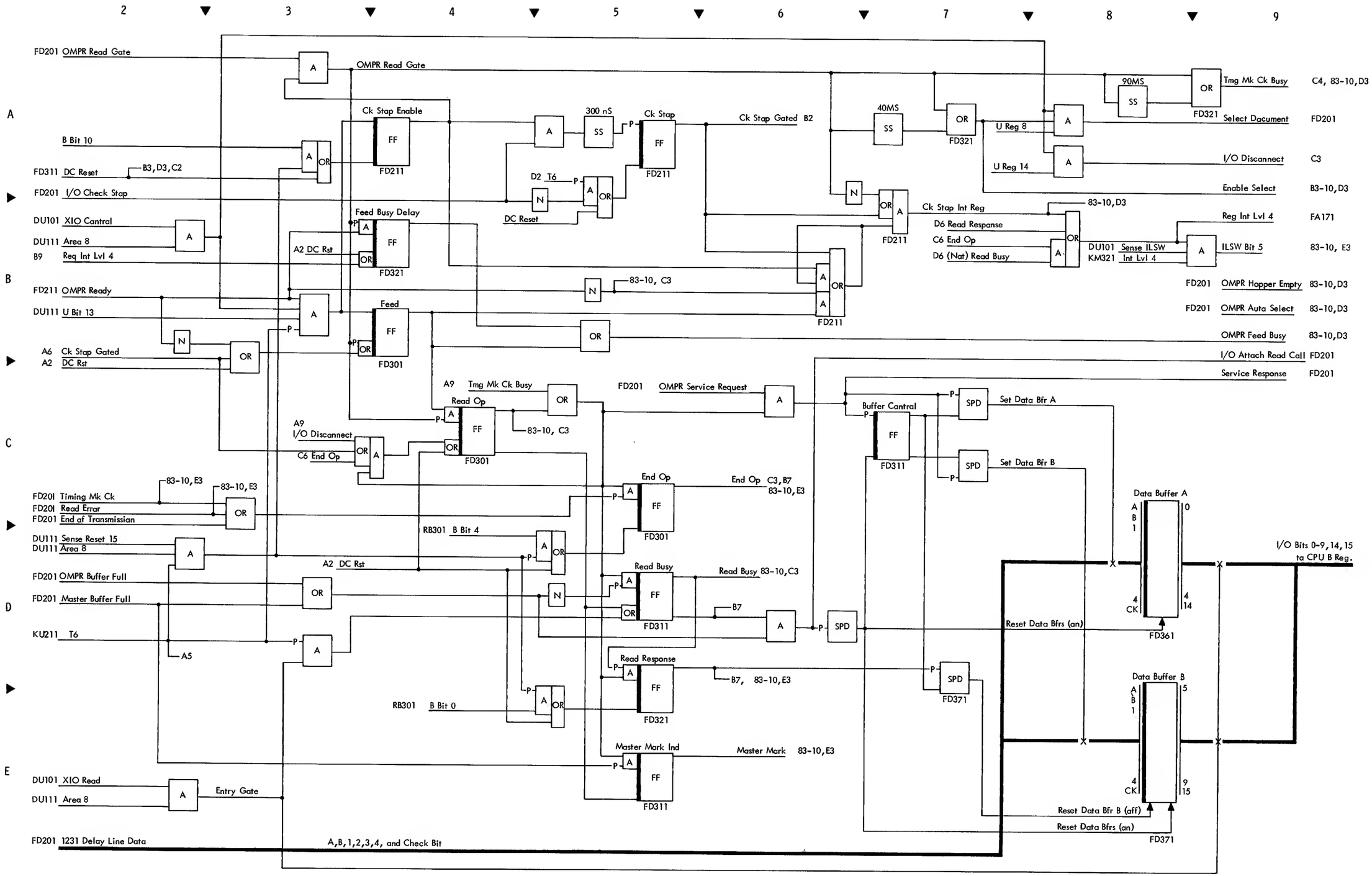


Diagram 84-10. 1231 OMPR Read

READER'S COMMENT FORM

1130 Features FEMDM SY26-4003-3

- How did you use this publication?

  As a reference source ☐
  As a classroom text ☐
  As..... ☐

- Based on your own experience, rate this publication...

As a reference source:	..... Very Good	..... Good	..... Fair	..... Poor	..... Very Poor
As a text:	..... Very Good	..... Good	..... Fair	..... Poor	..... Very Poor

- What is your occupation? .....

- We would appreciate your other comments; please give specific page and line references where appropriate. If you wish a reply, be sure to include your name and address.

- Thank you for your cooperation. No postage necessary if mailed in the U.S.A.

READER'S COMMENT FORM

1130 Features FEMDM SY26-4003-3

- How did you use this publication?

  As a reference source ☐
  As a classroom text ☐
  As..... ☐

- Based on your own experience, rate this publication...

As a reference source:	..... Very Good	..... Good	..... Fair	..... Poor	..... Very Poor
As a text:	..... Very Good	..... Good	..... Fair	..... Poor	..... Very Poor

- What is your occupation? .....

- We would appreciate your other comments; please give specific page and line references where appropriate. If you wish a reply, be sure to include your name and address.

- Thank you for your cooperation. No postage necessary if mailed in the U.S.A.

YOUR COMMENTS, PLEASE. . .

Your answers to the questions on the back of this form, together with your comments, will help us produce better publications for your use. Each reply will be carefully reviewed by the persons responsible for writing and publishing this material. All comments and suggestions become the property of IBM.

Note: Please direct any requests for copies of publications, or for assistance in using your IBM system, to your IBM representative or to the IBM branch office serving your locality.

Fold

Fold

FIRST CLASS
PERMIT NO. 110
BOCA RATON, FLA
33432

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

POSTAGE WILL BE PAID BY . . .

IBM Corporation
General Systems Division
Boca Raton, Florida 33432

Attention: Product and Programming Publications, Department 707

Fold

Fold

IBM

International Business Machines Corporation
Field Engineering Division
112 East Post Road, White Plains, N. Y. 10601

Cut Along Line

SY26-4003-3

YOUR COMMENTS, PLEASE. . .

Your answers to the questions on the back of this form, together with your comments, will help us produce better publications for your use. Each reply will be carefully reviewed by the persons responsible for writing and publishing this material. All comments and suggestions become the property of IBM.

Note: Please direct any requests for copies of publications, or for assistance in using your IBM system, to your IBM representative or to the IBM branch office serving your locality.

Fold

Fold

FIRST CLASS
PERMIT NO. 110
BOCA RATON, FLA
33432

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

POSTAGE WILL BE PAID BY . . .

IBM Corporation
General Systems Division
Boca Raton, Florida 33432

Attention: Product and Programming Publications, Department 707

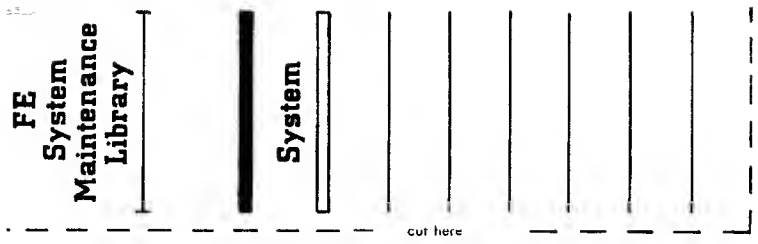
Fold

Fold

IBM

International Business Machines Corporation
Field Engineering Division
112 East Post Road, White Plains, N. Y. 10601

Cut Along Line



SY26-4003-3

IBM 1130 Printed in U. S. A. SY26-4003-3

IBM

International Business Machines Corporation
Field Engineering Division
112 East Post Road, White Plains, N. Y. 10601